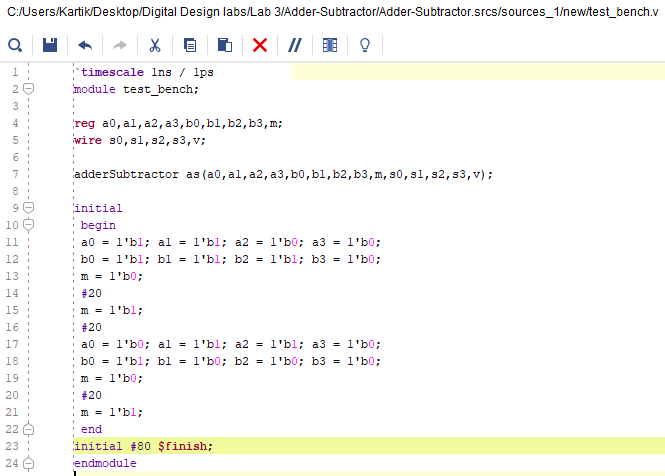
**(EEL2020)** **DIGITAL DESIGN LAB3 REPORT**

KARTIK CHOUDHARY B20CS025

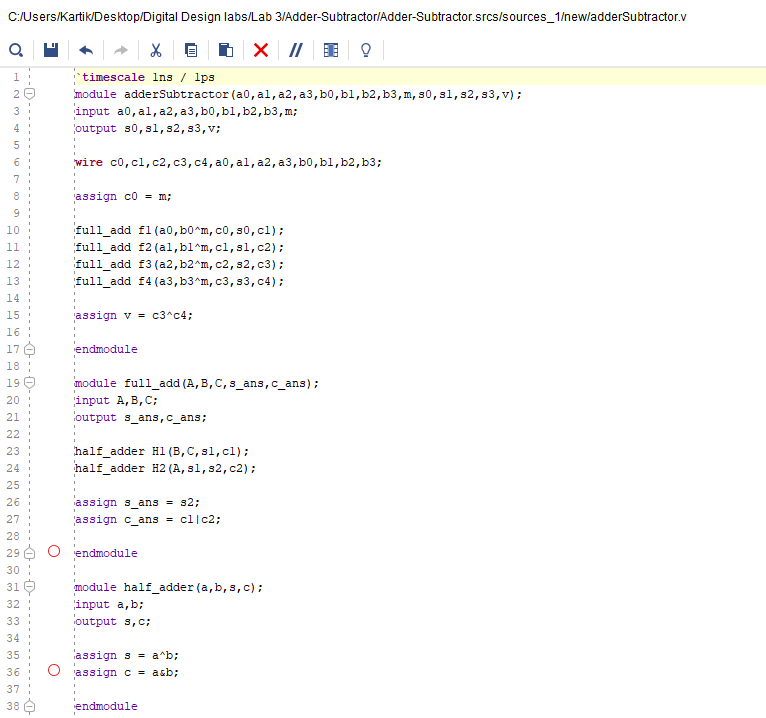
**Work 1:** **Modify the Four Bit Adder created in Lab 1 to implement an Adder-Subtractor Unit.**

a) Indicate overflow  
b) Modify the unit to implement a comparator.  
c) Test using the test benches

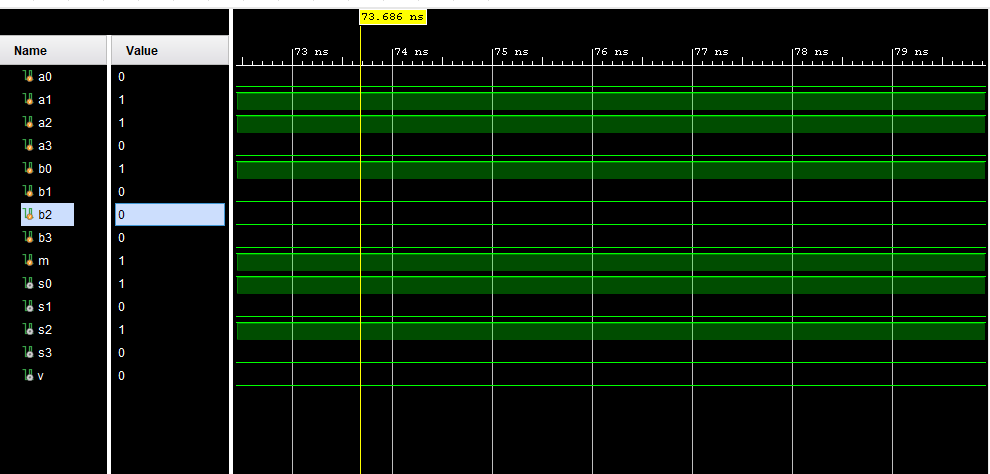
*Test bench*

**

*Verilog Code*

**

*Waveform*

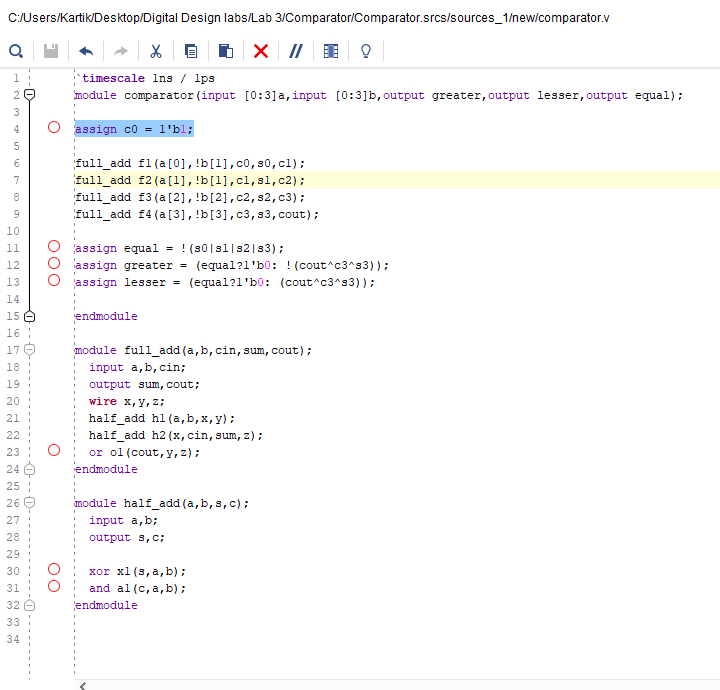


COMPARATOR

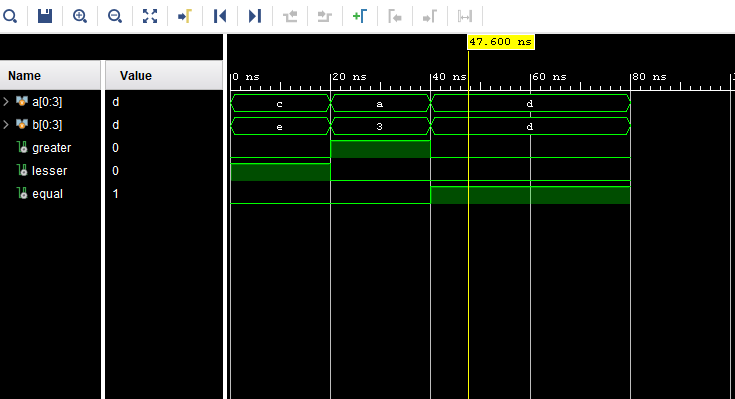
*Test Bench*

**

*Verilog Code*

**

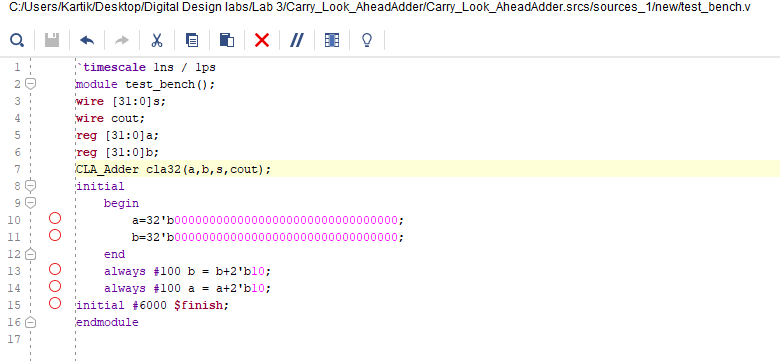
*Waveform*

**

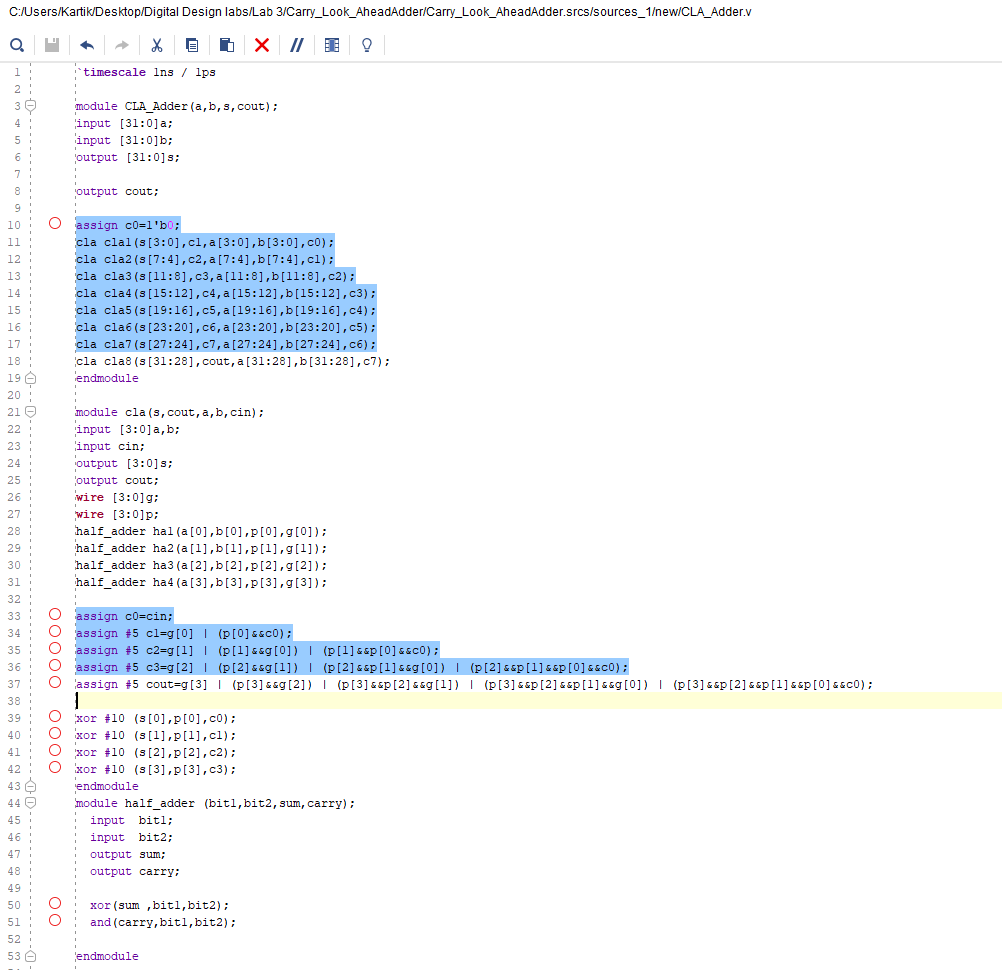
**Work 2: Write a Program to Implement the following Fast Adders [32 bit]**

a) Carry Look Ahead Adder

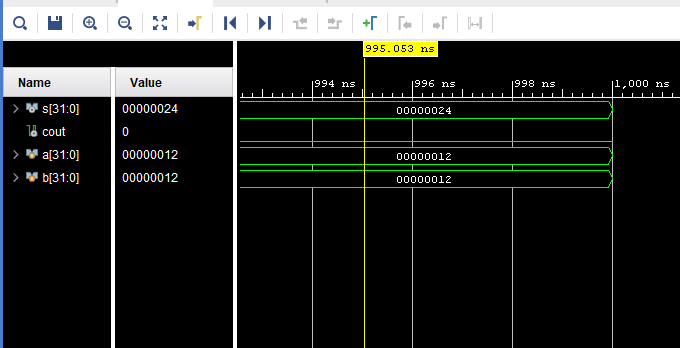
*Test Bench*

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*Verilog Code*

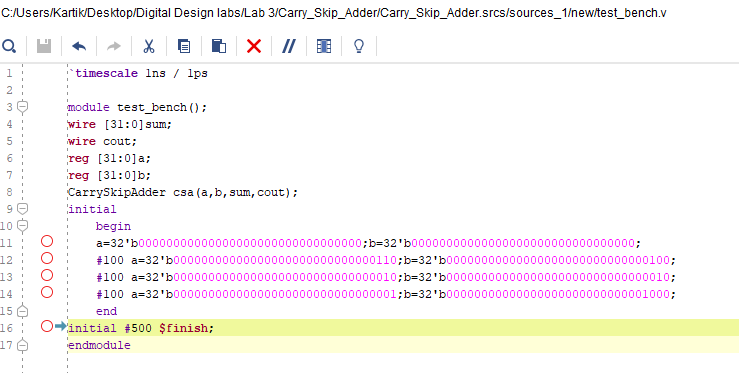
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*Waveform*

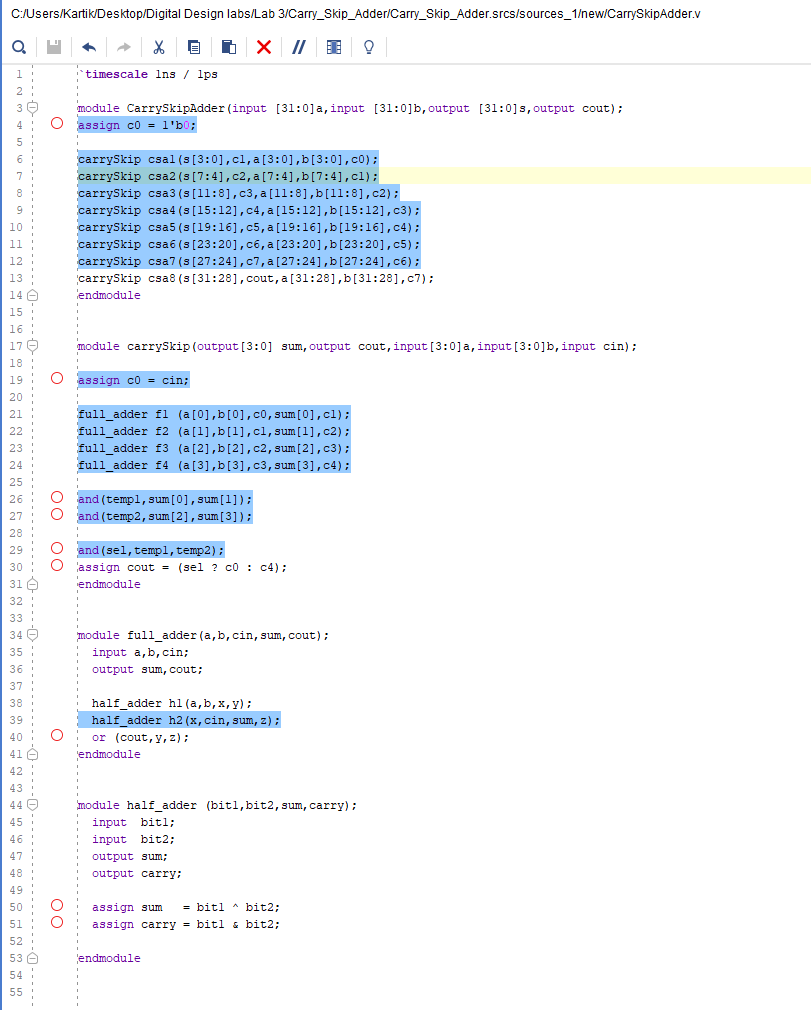
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b) Carry Skip Adder

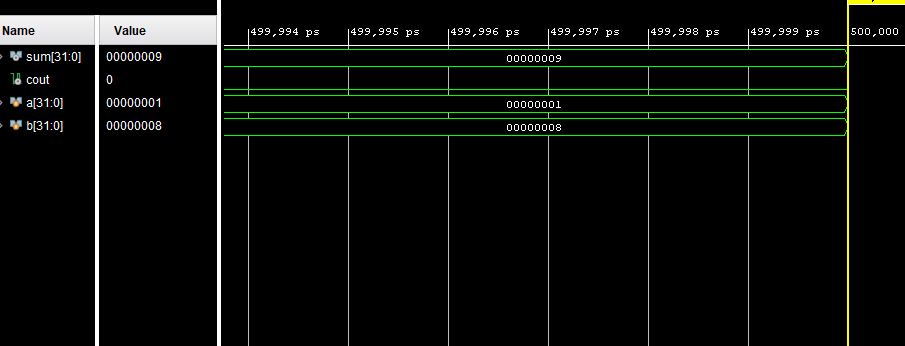
*Test bench*

**

*Verilog Module*

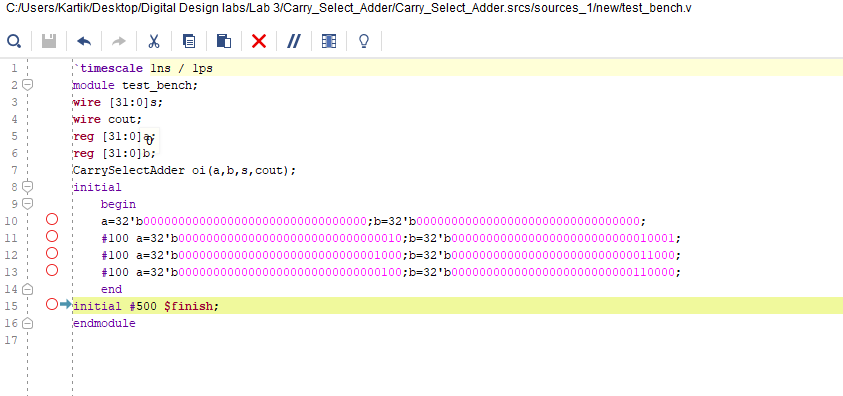
**

*Waveform*

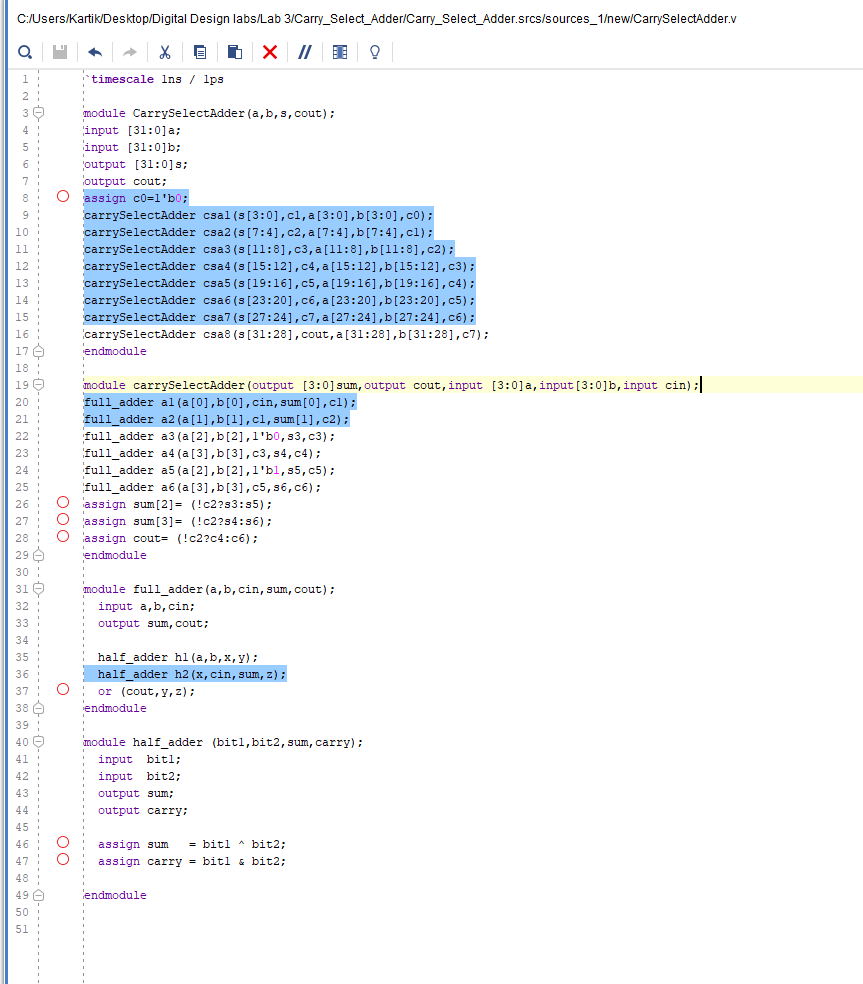
**

c) Carry Select Adder

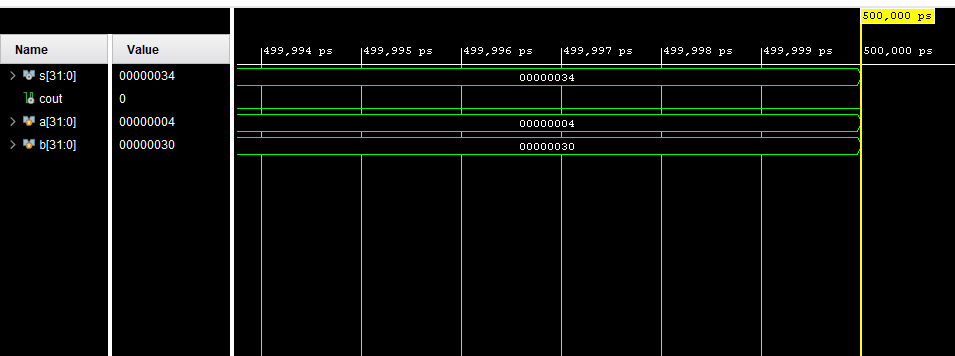
*Test Bench*

**

*Verilog Module*

**

*Waveform*

**